What is claimed is:

CLAIMS

1. A hysteresis circuit, comprising:

first, second, third, fourth and fifth CMOS transistors;

sixth, seventh, eighth, ninth and tenth CMOS transistors of a type complementary to the first five CMOS transistors;

an input terminal coupled to gates of said first, second, sixth and seventh CMOS transistors for applying an input signal;

an output terminal coupled with gates of said fourth and ninth CMOS transistors, and with drains of said fifth and tenth CMOS transistors for generating an output signal;

a first resistor coupled with sources of said seventh and ninth CMOS transistors, and source of said seventh CMOS transistor being connected to drain of said ninth CMOS transistor;

a second resistor coupled with sources of said second and fourth CMOS transistors and to ground, and drain of said fourth CMOS transistor being connected to source of said second CMOS transistor;

drain of said second CMOS transistor being connected to sources of said first and third CMOS transistors;

gates of said third, fifth, eighth and tenth CMOS transistors being interconnected, and being connected to drains of said first and sixth CMOS transistors; and

sources of said sixth and eighth CMOS transistors being interconnected, and drain of said eighth CMOS transistor and source of said fifth CMOS transistor being connected to ground.

2. The hysteresis circuit according to claim 1, wherein said first, second, third, fourth and fifth CMOS transistors are N-channel transistors.

3. The hysteresis circuit according to claim 1, wherein said sixth, seventh, eighth, ninth and tenth CMOS transistors are P-channel transistors.

4. The hysteresis circuit according to claim 1, wherein said first resistor is variable.

5. The hysteresis circuit according to claim 4, wherein said first resistor is linearly variable.

6. The hysteresis circuit according to claim 4, wherein said first resistor is non-linearly variable.

7. The hysteresis circuit according to claim 1, wherein said second resistor is variable.

8. The hysteresis circuit according to claim 7, wherein said second resistor is linearly variable.

9. The hysteresis circuit according to claim 7, wherein said second resistor is non-linearly variable.

10. The hysteresis circuit according to claim 1, wherein said fourth and ninth CMOS transistors are feedback transistors.

11. The hysteresis circuit according to claim 1, wherein said input terminal is at a low voltage level.

12. The hysteresis circuit according to claim 1, wherein said input terminal is at a high voltage level.

13. An integrated hysteresis circuit, comprising:

a substrate containing first, second, third, fourth and fifth CMOS transistors thereon;

sixth, seventh, eighth, ninth and tenth CMOS transistors of a type complementary to the first five CMOS transistors;

an input terminal coupled to gates of said first, second, sixth and seventh CMOS transistors for applying an input signal;

an output terminal coupled with gates of said fourth and ninth CMOS transistors, and with drains of said fifth and tenth CMOS transistors for generating an output signal;

a first resistor coupled with sources of said seventh

and ninth CMOS transistors, and source of said seventh CMOS transistor being connected to drain of said ninth CMOS transistor;

a second resistor coupled with sources of said second and fourth CMOS transistors and to ground, and drain of said fourth CMOS transistor being connected to source of said second CMOS transistor;

drain of said second CMOS transistor being connected to sources of said first and third CMOS transistors;

gates of said third, fifth, eighth and tenth CMOS transistors being interconnected, and being connected to drains of said first and sixth CMOS transistors; and

sources of said seventh and eighth CMOS transistors being interconnected, and drain of said eighth CMOS transistor and source of said fifth CMOS transistor being connected to ground.

14. The integrated hysteresis circuit according to claim 13, wherein said first, second, third, fourth and fifth CMOS transistors are N-channel transistors.

15. The integrated hysteresis circuit according to claim 13, wherein said sixth, seventh, eighth, ninth and tenth CMOS transistors are P-channel transistors.

16. The integrated hysteresis circuit according to claim 13, wherein said first resistor is variable.

17. The integrated hysteresis circuit according to claim 13, wherein said second resistor is variable.

18. A method on an electronic circuit, comprising:

generating hysteresis while decreasing high-current region and power consumption of an electronic device.

19. The method according to claim 14, further comprising:

limiting "through current" of the device when the device is switching with resistors and feedback transistors.

20. The method according to claim 15, further comprising:

adjusting the hysteresis by altering the resistance of the resistors.

21. A hysteresis circuit, comprising:

first, second, and third CMOS transistors;

fourth, fifth, and sixth CMOS transistors of a type complementary to the first, second, and third CMOS transistors;

an input terminal coupled to gates of said first and fourth CMOS transistors for applying an input signal;

an output terminal coupled with gates of said second and fifth CMOS transistors, and with drains of said third

and sixth CMOS transistors for generating an output signal;

a first resistor coupled across a source and drain of said second transistor, and sources of said first and third CMOS transistors being coupled to a drain of said second CMOS transistor;

a second resistor coupled across a source and drain of said fifth CMOS transistor, and sources of said fourth and sixth CMOS transistor being coupled to a drain of said fifth CMOS transistor;

gates of said third and fifth CMOS transistors being interconnected, and being connected to drains of said first and fourth CMOS transistors.

22. The hysteresis circuit according to claim 21, wherein said first, second, and third CMOS transistors are N-channel transistors.

23. The hysteresis circuit according to claim 21, wherein said fourth, fifth, and sixth CMOS transistors are P-channel transistors.